Radiation 1 ;valuation of an Advanced 64Mb 3.3V DRAM and insights into the Effects of Scaling on Radiation Hardness

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ABSTRACT -- In this paper, total ionizing dose radiation evaluations of the Micron 64 Mb 3.3 V, fast page mode DRAM and the IBM LUNA-ES 16 Mb DRAM are presented. The effects of scaling on total ionizing dose radiation hardness are studied utilizing test structures and a series of 16 Mb DRAMs with different feature sizes from the same manufacturing line. General agreement was found between the threshold voltage shifts of 16 Mb DRAM test structures and the threshold voltage measured on complete circuits using retention time measurements. Retention time measurement data from early radiation doses are shown that allow internal failure modes to be distinguished.

I. INTRODUCTION

Advances in DRAM density and performance continue to occur. Currently, densities of 1Gb are being achieved in advanced prototype DRAMs [1-2]. Design rules for these advanced DRAMs are 0.25 µm or less with submicron cell areas. As device geometry shrinks, power supply voltage must be reduced and new circuit design approaches must be used in order to maximize performance benefits from scaling. These changes affect the radiation hardness of these circuits with complex effects that are often difficult to predict from basic responses of MOS transistors.

Unlike conventional CMOS circuits, DRAMs are very sensitive to small changes in threshold voltage, making them inherently more sensitive to ionizing radiation. However, the reduced oxide thickness of newer generation devices has improved their radiation hardness, and DRAMs continue to gain acceptance for critical space flight applications. Cassini, Mars Pathfinder, Clementine, Mars Global Surveyor, and Pluto Express are examples of space projects that used, are using, or are exploring the use of large DRAM arrays. DRAMs are frequently used in solid state recorders (SSRs) where large amounts (> 1 Gb) of minimum power memory are required. DRAMs may also be suitable for computer main memory as evidenced by their selection for Mars Pathfinder's flight computer. DRAMs are also useful test vehicles for the evaluation of radiation effects in scaled MOS devices because they lead the industry in device scaling and density.

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In earlier work we showed that retention time was a useful circuit-level diagnostic parameter to evaluate total dose degradation of DRAMs [3]. Results of the earlier work showed that there was no clear relationship between device scaling and radiation tolerance for DRAMs with 0.5 to 0.8 µm feature sizes. This was probably due to differences in design, such as the use of multi divided array structures, which affect the internal design tolerance for changes in threshold voltage of internal transisters, as well as differences in field oxides. However, there is a general trend towards lower total ionizing dose tolerance for devices with reduced supply voltages, which is important not only for conventional total dose effects, but also for microdose errors in individual cells from single interactions of heavy ions [4-6]. In the present work we develop the use of DRAM retention time as a diagnostic tool and use it to build a relationship between DRAM cell response and radiation damage.

II. EXPERIMENTAL APPROACH

All devices were irradiated with a Shepherd model 81-24 ^{60}Co room type irradiator, at 1.0-65 rad(Si)/s at room temperature. Source calibration was done using a MDH Industries ion chamber. Electrical measurements on DRAM circuits were performed with an ADVANTEST T3342 VLSI test system. Test structures were measured with a Hewlett-Packard 4062C parametric measurement system. Retention time measurements were made by writing to a specific memory cell location, waiting for a specific time before refreshing, and then determining whether data stored in that location was still valid. A set-its of measurements were made in order to determine the maximum time delay between the write and refresh cycle for *each* location. This measurement is very time consuming, particularly for unirradiated devices, which often have maximum refresh delays of more than 100 seconds. Less time is required for irradiated devices because the refresh interval decreases with radiation. The result of these measurements is a distribution of retention times for all measured cells. These are distributions, not single values, primarily because of cell-to-cell variations in threshold voltage from fluctuations in the number and spatial distribution of dopant atoms [7, 8].

Dynamic bias was maintained on all DRAMs during irradiation. Dynamic bias applies a clock signal periodically refreshing each cell location. However, the time required for refresh is very short compared to the interval between successive refresh cycles so that individual access transistors are essentially biased statically. In-situ measurements were made of

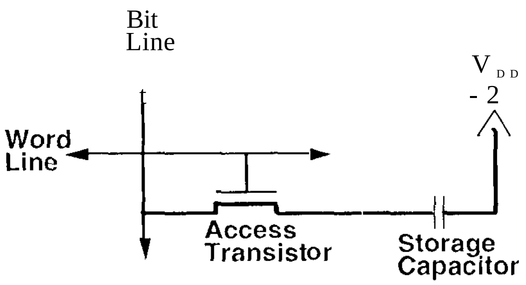

Figure 1. Simplified schematic of DRAM cell.

standby supply current, operating supply current, output drive current, and functionality at selected time intervals. Complete measurements of electrical performance, including special measurements of each cell's minimum data retention time, were performed at selected doses.

Bias on the access transistor in normal operation can be deduced from Figure 1, Because both the reference plate of the capacitor and the bit line (which connects to a sense amp) are held at half V_{dd} and the gate is off, i.e. 0 V, maximum bias across the gate occurs when the capacitor stores $+V_{dd}$. Note that the direction of the electric field drives trapped holes *away* from the Si-SiO_2 interface which reduces the fraction of trapped holes, Test structures were irradiated under static bias, using several different bias conditions in order to compare total dose damage in these highly scaled devices with existing data on devices with larger feature size.

Several high density DRAMs and a DRAM test structure were used for this work. The Micron 16 Mb, 5 V/3.6 V DRAM is an example of a mature 16 Mb device which has evolved from earlier process modifications. This device requires a 5 V external power supply but uses an on-chip regulator to reduce the memory array supply voltage to 3.6 V. It is configured as a 4 M-address by 4-bit memory array and uses 0.67 μm design rules. Also tested for this work was a more advanced product, the Micron 64 Mb, 3.3 V, fast page mode DRAM configured as a 16 M-address by 4-bit array. It is fabricated using 0.37 μm design rules and has an 11 nm access transistor gate oxide thickness. Some caution should be used in interpreting the 64 Mb DRAM data because it was tested early in its product cycle and is more of a working prototype than a production device, Also tested was the IBM LUNA-ES 16 Mb DRAM which, like the Micron 16 Mb DRAM, uses a 5 V/3.6 V external/internal regulated voltage arrangement and is configured as a 4 M-address by 4-bit memory array. The test structures used for this work were Micron process control monitors from the 16 Mb 5 V/3.6 V DRAM process. These test structures are set up with all gates tied to a single package pin. The source, drain, and the body contacts are common to all measured devices. To access a particular transistor, only the drain contact need be changed, once the other contacts have been made. N-channel transistors used on these test structures are representative of memory cell access devices with the same geometry, design rules, and oxide thicknesses of the 5 V/3.6 V Micron DRAMs. Additional information for the devices and test vehicles used for this work are included in Table I. The Micron 4 Mb DRAM which had been previously tested [3] is included and allows scaling comparisons across three full generations of the same manufacturer's devices. Note that the thicknesses of both the gate and field oxides are reduced as they are scaled to smaller dimensions.

Table I. Description of Test Devices

Device Type	Voltage	Access Device Dimensions	Cell Area μm^2	Gate t_{OX}	Field t_{OX}
4Mb DRAM	5.0V	-/0.75		19nm	
16Mb Test Structures	3.6V*	0.80 1/0.)75	N/A	15nm	340nm
16Mb DRAM	3.6V*	0.864/0.675	1.01	15nm	340nm
16Mb DRAM	3.3V	0.78/0.61	0.82	15nm	3.1(111111
64Mb DRAM	3.3V	0.4/0.37	0.656	11nm	240nm
16Mb IBM Luna-ES	3.6V*				

Notes: Gate t_{OX} is for DRAM memory cell access devices. * Denotes external supply voltage of 5.0V. Dashes denote where information was not available.

III. EXPERIMENTAL RESULTS

A. *Micron 64 Mb, 3.3 V DRAM*

The Micron 64 Mb 3.3 V DRAM was irradiated at 10 rad(Si)/s while dynamically biased. in-situ measurements of dynamic supply current, standby supply current, input leakage current high, and functionality with error count were taken using a 10 foot cable that allowed full test capabilities at the device under test.

The dose response of standby supply current for a Micron 64 Mb, 3.3 V device is shown in Figure 2. The standby current started out at about 500 μA and increased only slightly at levels

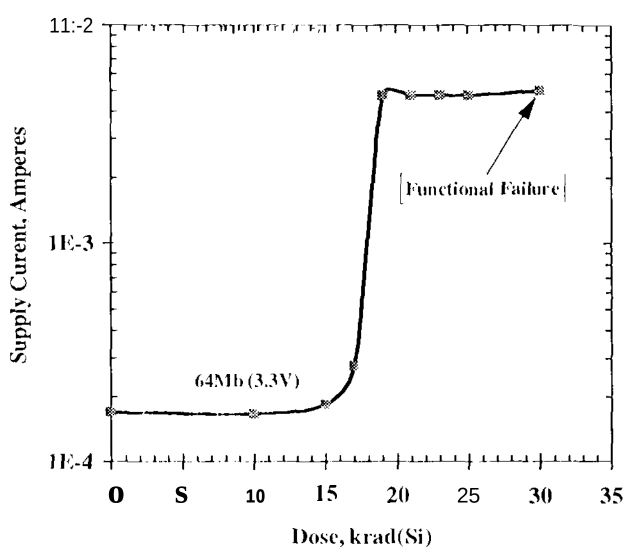

Figure 2. Response of standby supply current for the Micron 64Mb DRAM. Note the sharp increase in supply current after 15 krad(Si).

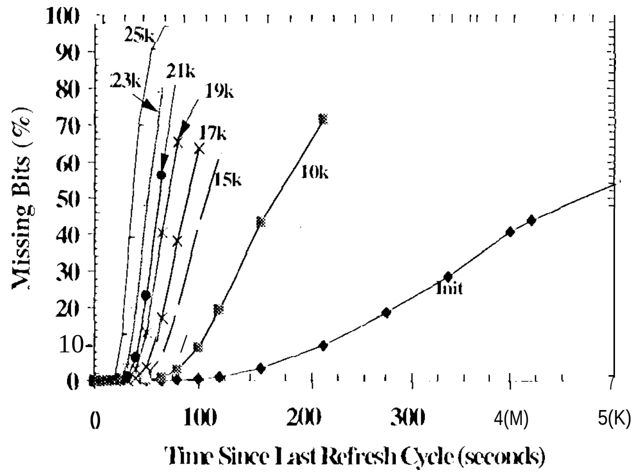

Figure 3. Retention time data for the Micron 64Mb DRAM. Note the large changes in retention time at 10 and 15 krad(Si).

below 15 krad(Si). Above 15 krad(Si), it increased rapidly to about 4 mA by 19 krad(Si) and did not increase further at higher radiation levels. This differs from conventional data for MOS circuits that fail from field oxide inversion which exhibit a steady increase in supply current at levels of radiation above the point where inversion occurs [9]. This device continued to operate at higher levels of radiation without significant further current increases until it failed functionally at 30 krad(Si). A second sample behaved similarly, but failed functionally only a few krad(Si) after the rapid current increase.

Retention time measurements were also made on the 64 Mb device (see Figure 3) which behaved similarly to older DRAMs. In Figure 3, the x-axis is the time in seconds since the last refresh cycle (or row access) was initiated. The y-axis is the percentage of the 64M bits whose data was not retained, so called lost bits. The entire 64 Mb array was monitored for this measurement so that the 50% point (or median) in Figure 3 corresponds to the time when half the 64M cells had lost their data. Note the overall shift to shorter retention times as radiation dose increases as well as the sharp slope increase in the retention time curve. Changes in retention time are caused by increase in leakage current, either from the access transistors or the storage capacitors.†

Comparing figures 2 and 3, it is clear that the power supply circuit and cell leakage behave in different ways during irradiation. The abrupt step in supply current occurs at approximately 17 krad(Si), but no hint of such a change is observed in the retention time results, which continue to change in a smooth, predictable way well beyond the 17 krad(Si) transition point for power supply current. This shows that the large increase in supply current cannot be caused by changes in leakage in the critical memory cell regions, but must be due to changes in other regions of the device, such as the input/output circuitry or substrate bias generator. This example illustrates one way in which retention time can be used to gain increased understanding of response mechanisms for DRAMs. Later in the paper, the relationship between device retention time distribution and the subthreshold response of test structures will be explored.

Previous work [3] pointed out that DRAMs exhibit two classes of supply current degradation. In the first class of degradation a rapid increase in supply current occurs followed by functional failure. Figure 4, which compares the standby current responses of the various Micron devices, shows both types of current degradation. This first class of current degradation is believed to be field oxide inversion accounting for the excessive current. The functional plateau of the 64 Mb data at the high total dose levels is not totally consistent because field leakage should continue to increase with dose, not level off. Thus, the internal mechanism for the 64 Mb device may be different.

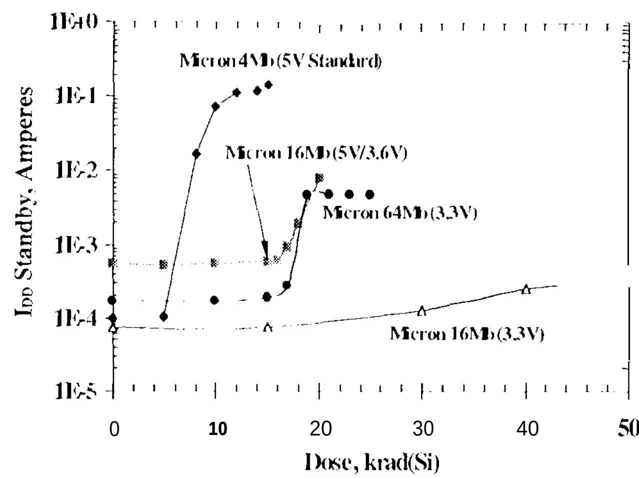

Figure 4 Supply current as a function of cumulative dose for several Micron high density DRAMs. Two differing damage mechanisms are clear a rapid increase and a more gradual one, corresponding to field oxide leakage and gate oxide leakage, respectively.

The second type of current degradation, a more gradual increase with total dose, is shown in Figure 4 for the shrunk Micron 16 Mb device. As is typical for devices exhibiting gradual current increases, functional failure occurred at a substantially higher total dose. This more gradual degradation is believed to be caused by subthreshold leakage increases in the access devices of the memory cells; test structure test data, discussed in a later section, corroborates this assumption).

B. Retention Time Analysis

DRAM retention time measurements can provide indirect information about *changes* in the threshold voltage of internal

†Figure 3 shows that the slope of the retention time decreases with increasing levels of radiation. As the radiation level increases, the retention time is dominated by global changes in threshold voltage due to radiation, and statistical differences in threshold voltage of individual transistors have less relative effect on retention time. Evaluation of retention time curves for different radiation levels shows that the distribution of threshold voltage variations is essentially unchanged by radiation.

transistors provided certain assumptions are valid, namely that the primary source of leakage current in the DRAM storage element is subthreshold leakage in the access transistor. The threshold voltage that applies here corresponds to the very low current region -- ~ 10^{-12} A -- of the device characteristics because the DRAM cells are essentially off during normal operation. Thus, changes in retention time are proportional to changes in current through the access transistors in the deep subthreshold region. Note that although V_{ot} and V_{it} work in opposite directions for n-channel transistors at high currents, this is not true for the low current region that is important in DRAMs. In the deep subthreshold region, the transistors operate near the midgap region where all changes in V_{it} have negligible effect. Thus, at very low currents threshold voltage changes are essentially due only to changes in the V_{ot} component.

Changes in subthreshold current and in the subthreshold slope of the I-V curve can be related to changes in threshold voltage by Equation 1:

$$\ln\left(\frac{I_2}{I_1}\right) = m_2 V_{T2} - m_1 V_{T1} \qquad (1)$$

where I_1 and I_2 are the subthreshold currents at two dose levels, m_1 and m_2 are the subthreshold slopes, and V_{T1}, and V_{T2} are the threshold voltages.

In the deep subthreshold region, the current is so low that changes in subthreshold slope have only a slight effect on the I-V characteristics, and the subthreshold slope is dominated by ΔV_{ot}. With this assumption, changes in current occur because of changes in V_{ot}. Changes in the retention time can then be related to total dose using the t_{ox}^2 dependence expected for gate oxide shifts [10]. With the additional assumption that retention time is proportional to the reciprocal of subthreshold current, these relationships can be combined to yield Equation 2:

$$\ln\left(\frac{\tau_1}{\tau_2}\right) = (3.6\text{x}10^{-4})\, t_{ox}^2\, m\eta D \qquad (2)$$

where: τ_1 and τ_2 are the initial and post-rad retention times, η is the hole trapping efficiency, D is the dose in krad(Si), and t_{ox} is expressed in nm.

This relationship holds for each pass transistor in the memory array. Before irradiation there is a distribution of retention times that occurs because of initial threshold voltages variations. After irradiation this distribution is still present, but it is superimposed on the change in threshold voltage. As discussed below, once ΔV_{T} becomes much larger than the differences in the initial distribution of threshold voltages, the effect of these fluctuations on retention time is reduced. This causes the slope of the retention time distribution to increase after irradiation.

Retention time distributions prior to irradiation can be used to evaluate the distribution of threshold voltages on the entire

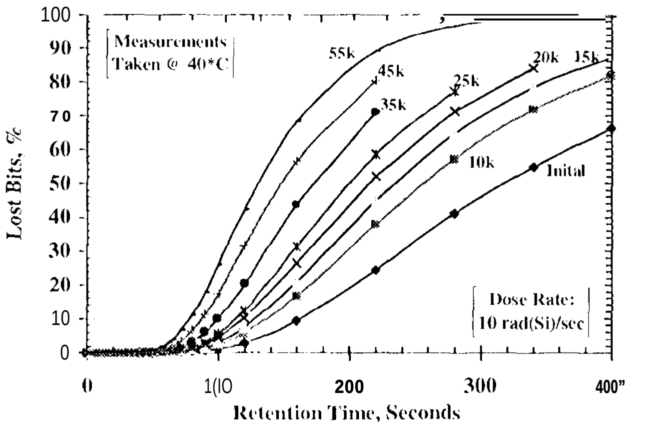

Figure 5. Retention time curves for an IBM LUNA-ES 16Mb DRAM at selected total dose levels (in krad(Si)).

DRAM array. The initial distribution of retention times in Figure 5 corresponds to a standard deviation of approximately 8 mV in threshold voltage. If we assume that the nominal threshold voltage is 0.7 V, this corresponds to a threshold fluctuation of 7 mV for the distribution of devices on the entire chip, using Equation 1 and assuming that all devices have the same subthreshold slope (slight differences in slope will have little effect in the low current region). This compares closely with calculations of the effect of doping fluctuations on threshold voltage of +/- 9 mV for 0.6 µm devices [7]. Evaluating the standard deviation of V_T at different radiation levels shows that it is essentially unchanged, leading to the conclusion that the threshold shift after irradiation is nearly identical for all the transistors within the array, and that the statistical spread in V_T is unaffected by radiation damage.

The effective threshold voltage can be extracted from median values of normalized retention times like those shown in Figure 6. Note that the slope is nearly constant, which corresponds to the case where oxide traps dominate the threshold

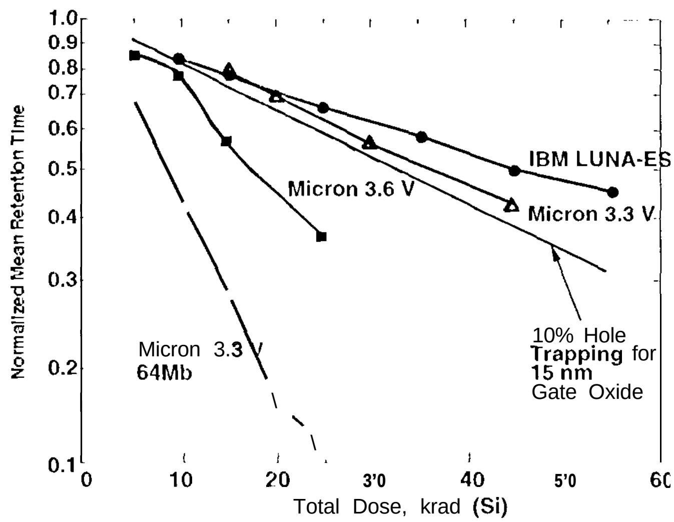

Figure 6 Median normalized retention time vs. dose for several DRAMs Note the decreased hole trapping indicated by reduced slope for each DRAM as scaling increases

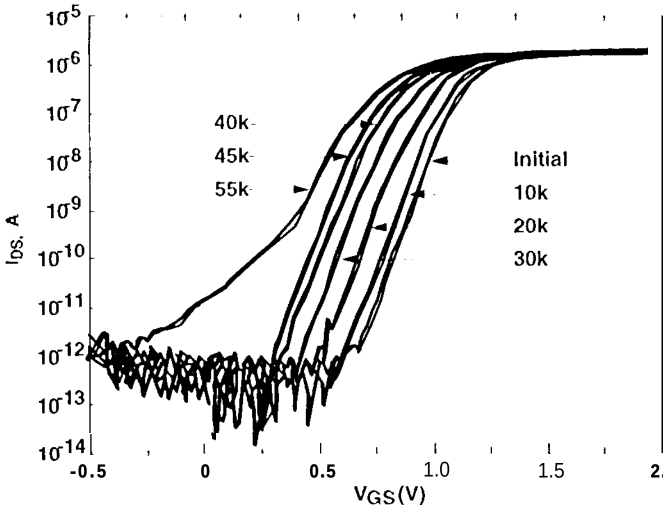

Figure 7. Subthreshold curves for the 16Mb 3.6V DRAM test structure. The large distortion at 55 krad(Si) is due to field oxide leakage.

voltage response. All three 16 Mb devices have similar slopes, and correspond to about 10% hole trapping for oxide thicknesses of 15 nm; the low yield of trapped holes is due to the direction of the electric field. The test structure results corroborate this interpretation. The 64 Mb device also exhibit a smooth regular change in retention time with total dose, but the magnitude of the change is larger than for the 16 Mb devices.

Figure 7 shows a subthreshold plot for a test structure from the 16 Mb 5 V/3.6 V process. The curves have a nearly constant slope which shows that hole traps dominate the response. The large increase in subthreshold current at the highest dose of 55 krad(Si) is due to field oxide leakage in the device.

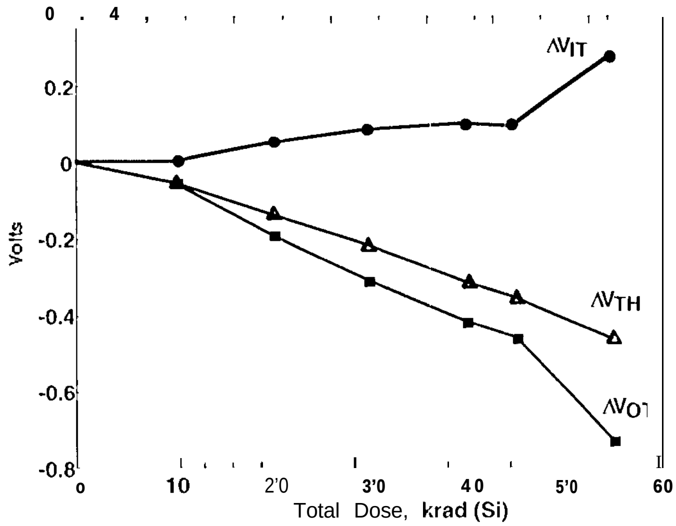

Figure 8. Threshold voltage and charge separation for the 16 Mb 3.6V DRAM test structure. Note that this test structure exhibits typical behavior under these conditions for an n-channel MOS device.

The test structure data of Figure 7 can be used to extract the interface trap and oxide trap components of the threshold shift, as shown in Figure 8. The interface trap component is approximately 10% of the hole trap contribution to threshold voltage shift. Figure 8 is a useful way to compare total dose damage on scaled devices internal to DRAMs with the results for other technologies. However, the threshold voltage in this figure corresponds to the conventional interpretation of threshold voltage in the strong inversion region (high drain current). As noted earlier, operation of a DRAM pass transistor corresponds more closely to the midgap region with currents below 10^{-11} A.

IV. Discussion

Test structures from Micron's 16 Mb 5 V/3.6 V DRAM line were irradiated under various bias conditions: 3.3 V, 1.8 V, and zero volts. Separate samples were used for each bias condition. The I-V curves were separated into hole trap and interface trap components using the subthreshold slope method [11]. Test structure data were then compared with data from fully functional 5 V/3.6 V 16 Mb Micron DRAMs.

The results of these tests are shown in Figures 9 and 10. In Figure 9, ΔV_{IT} is plotted for three gate biases as a function of dose. Note the increasing slope of ΔV_{IT} for increasing gate bias. The large increase in ΔV_{IT} at 55 krad(Si) in the 2 MV/cm curve results from an erroneous interpretation of ΔV_{IT} brought on by the field oxide leakage seen in Figures 7 and 8 at 55 krad(Si). Figure 10 plots ΔV_{OT} under the same gate bias conditions. Under high field conditions, nearly 100% of the holes are trapped. Reducing the bias causes less charge trapping, as expected.

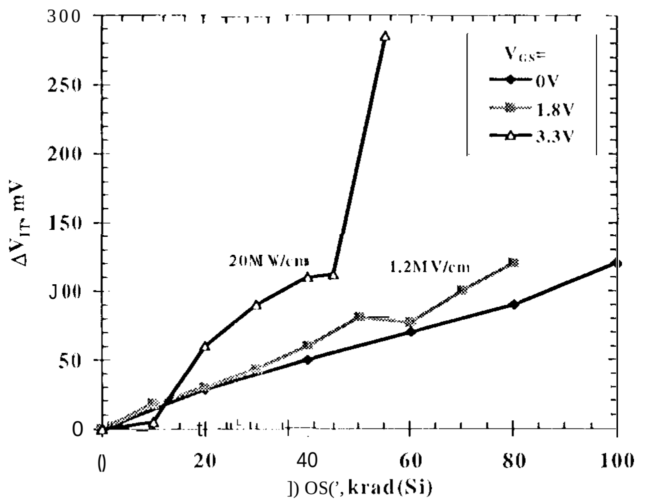

Figure 9. Change in voltage due to interface states for the Micron 5V/3.6V DRAM test structures under three gate biases.

The data in Figures 9 and 10 are in good general agreement with established data [12-14]. They corroborate the assumption that, at least for the process where test structures were available, small shifts in the threshold voltage of internal access transistors are the primary mechanism for changes in retention time. This is can be said because as threshold voltage

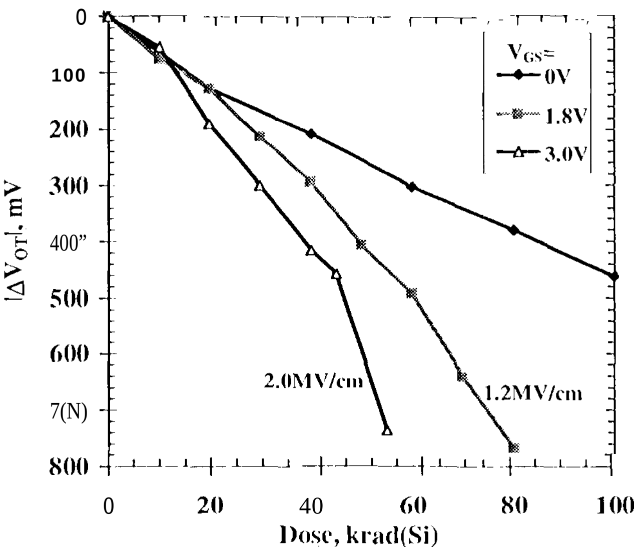

Figure 10. Change in voltage due to oxide trapped charge for the Micron 5V/3.6V DRAM test structures under three gate biases. Note that the 1.2MV/cm curve is the typical bias condition for this device under normal operating conditions.

shifts negatively while at the same time becoming more leaky. They also demonstrate the usefulness of retention time as a diagnostic tool for complex circuits. Retention-time measurements for the other 16 Mb DRAMs degraded in a very similar manner, and were consistent with the hole trapping expected for these oxide thickness under the bias conditions present in the DRAM array during normal operation.

Although results for the 16 Mb devices were consistent with the expected threshold voltage changes in access transistors, this may not always be the case, because DRAMs are complex circuits. Other factors, such as leakage in the capacitors, degradation of sense amplifiers, and field oxide inversion in other circuitry within the DRAM may also contribute to the overall response of these devices, as well as degradation of more global circuitry, such as internal supply voltage sources or substrate bias generators. Some of these mechanisms can be distinguished by testing DRAMs under different bias conditions. For example, storing complementary information in cells will change the voltage across the access transistor; this allows capacitor leakage to be distinguished from access transistor leakage, provided a bit map is available for the DRAM array. The temperature sensitivity of pre- and post-radiation retention time measurements can also be used to further distinguish between competing failure mechanisms because the temperature dependence of threshold voltage is well established.

Retention time measurements are useful why to determine the effect of ionizing radiation on the critical storage elements within these complex devices. In many cases they can be used to indirectly measure threshold voltage changes in the access transistors from external circuit pins, as well as the distribution of threshold voltages within very large circuits. Retention time measurements change in a smooth, predictable way with radiation at low radiation levels, and can be used as a precursor of some classes of failure mechanisms as well as to compare DRAMs from different manufacturers.

Comparing other parameters such as power supply current and functional operation with retention time data allows changes in the storage array to be distinguished from other failure modes. Thus, it is very useful as a diagnostic tool. For several of the DRAMs, this comparison showed that increases in power supply current at low radiation levels were not caused by leakage current or field-oxide inversion in the DRAM array because the retention time continued to exhibit small incremental changes with radiation well beyond the corner for large increases in operating current.

V. Summary

Ionizing radiation data have been presented for an advanced 64 Mb DRAM with a feature size of 0.4 μm. Measurements of retention time showed that the internal memory storage array degraded in a similar manner to that of older DRAMs with larger feature sizes, and that increases in power supply current were not caused by transistors within the array. Measurements of test structures from a 16 Mb DRAM process provided more direct corroboration of the dependence of retention time on small threshold voltage shifts in access transistors, and demonstrate the usefulness of this circuit level parameter for diagnostic purposes.

VI. Dedication

The first illltll(~l'01'lllis paper dedicates this work to Clifford B. Strew who died on July 4, 1995. He was a father who showed me the way in life and who, through his humor, patience and love showed me what it means to live life to its fullest. He will be remembered by many with much fondness. He is missed dearly.

VII. Acknowledgments

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